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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
STREGE, JOHN B	

ART UNIT	PAPER NUMBER
2625	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/986,299	HIROI ET AL.	
	Examiner	Art Unit	
	John B. Strege	2625	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 December 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *28-42* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *28-42* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *03 May 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Response to Amendment

In response to the Applicant's amendment received 12/3/04, all requested changes to the claims have been entered.

Applicant's arguments filed 12/3/04 regarding the provisional double patenting have been fully considered but they are not persuasive. Applicants argue that it is not proper in terms of a double patenting rejection to contend that method claims of one patent can be utilized to reject apparatus claims of another patent. However, it would be obvious to one of ordinary skill in the art of semiconductor inspection using image processing to develop a method given an apparatus or vice versa and therefore the rejection is respectfully maintained regarding the new claims.

Applicant's arguments with respect to the art rejections of claims 1-15 have been considered but are moot in view of the new ground(s) of rejection.

DETAILED ACTION

Double Patenting

1. Claims 28-30, and 38-39 are provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 29-30 and 37 of copending Application No. 09986577 in view of Gallarda et al. USPN 6,539,106 (hereinafter "Gallarda"). The instant application and application number 09986577 are obvious variations of each other (see for example claim 28 of the instant application and claim 29 of 09986577). For the mapping below the claims mentioned outside the parentheses correspond to the instant application and those inside the parentheses correspond to application 09986577.

Claim 28 discloses –

a pattern inspection method comprising the steps of (claim 29 discloses "a pattern inspection apparatus comprising" – it would have been obvious to one of ordinary skill in the art of image processing inspection to design the apparatus given the method)

attaining a digital image of an object substrate through microscopic observation thereof (claim 20 discloses "an image detecting part for detecting a digital image of an object substrate")

detecting defects of a pattern formed on said object substrate by comparing said digital image with a reference image stored in a memory while masking a pre-registered region or a pattern matching with a pre-registered pattern (claim 29 discloses a defect detecting means for detecting defects of the pattern formed on said object substrate by comparing the digital image attained by the image detecting means with a reference image while masking a pre-registered region or a pattern matching with a pre-registered pattern)

and outputting an image of a defect among the defects detected together with positional distribution data thereof on said object substrate on a display screen (claim 29 discloses output means for outputting data regarding the defects detected by the defect detecting means including digital images of said defects detected by masking and the postional distribution data thereof in a map form – although claim 29 uses the words "map form" for the output means, it would be obvious to one of ordinary skill in the art that a map is an effective way of outputting defect data and position).

Gallarda discloses outputting a defect map to a display with positional information of the defect (figure 3 numeral 345), thus Gallarda is outputting an image of a defect together with positional information.

Gallarda, the instant application, and 09986577 are all analogous art because they are all from the same field of endeavor of using image processing to detect defects.

At the time of the invention it would have been obvious to one of ordinary skill in the art to output defect information and defect position information using a defect map. Thus it would have been obvious to one of ordinary skill in the art to devise the pattern inspection method of claim 28 of the instant application given the pattern inspection apparatus of claim 29 of application 09/986,577.

Claim 29 of the instant application maps to claim 30 of application 09986577.

Claim 30 is mapped to claim 31 of application 09986577.

Claim 38 is similar to claim 28 with the added limitations of extracting defects and classifying defects. Claim 37 of application 09986577 discloses defect extracting means and defect classifying means.

Claim 39 is obvious over Gallarda who displays the defect type (figure 3, numeral 345).

This is a provisional obviousness-type double patenting rejection.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claim 38 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 38 line 11 discloses "classifying the defect which image is displayed on said display screen." This appears to be a grammatical error, however it obscures the meaning of the limitation. For examining purposes the Examiner will read the limitation as classifying the defect which is displayed on said display screen."

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claims 28-29,38-39 are rejected under 35 U.S.C. 102(e) as being anticipated by Gallarda et al. USPN 6,539,106 (hereinafter "Gallarda").

Regarding claim 28, Gallarda discloses a pattern inspection method comprising the steps of: attaining a digital image of an object substrate through microscopic observation thereof (col. 3 lines 23-29, and col. 16 lines 27-34 disclose that the test image can be from a scanning-electron-microscope); detecting defects of a pattern formed on said object substrate by comparing said digital image with a reference image stored in a memory while masking a preregistered region or a pattern matching with a pre-registered pattern (col. 3 lines 19-55 disclose preparing a reference image and a test image, extracting features from the reference image and extracting features from the test image, and comparing features of the reference image and of the test image to identify defects, wherein the extracting features from an image can comprise matching a feature template in the image and identifying features in the image that match the feature-template [masking],); and outputting an image of a defect amont the defects detected together with positional distribution data thereof on said object substrate on a display screen (figure 3 numeral 345 discloses a display for outputting a defect map, defect location, size, type, etc.).

Regarding claim 29, Gallarda discloses that the reference image and test image can be obtained using a scanning-electron-microscope (col. 16 line10-34) and a feature template can be used to aid in the feature extraction for a particular type of image can be used to extract the features (col. 17 lines 45-59), thus it is inherent that if the feature template is to be used with a microscopic reference and test images then it must be set up using a microscopic image.

Regarding claim 38, Gallarda discloses a pattern inspection method comprising the steps of: attaining a digital image of an object substrate through microscopic observation thereof (col. 3 lines 23-29, and col. 16 lines 27-34 disclose that the test image can be from a scanning-electron-microscope); detecting candidate defects by processing the attained digital image (the image is processed by matching features of the test image to the reference image); extracting defects form the detected candidate defects by excluding candidate defects located in a predefined region on the object substrate or having a pattern that matches with a pre-registered pattern (col. 3 lines 53-55); displaying an image of a defect among the extracted defects on a display screen together with postional distribution data on the object substrate and feature quantity data thereof (figure 3 numeral 345 discloses a displaying a defect map, defect location, size, type etc.), classifying the defect which is displayed on said display screen (figure 3 numeral 345 discloses the type of defect [classification] is displayed); outputting class data of the classified defect together with feature quantity data thereof (figure 3 numeral 340 discloses outputting the defect size and type to memory).

Regarding claim 39, class data (type) of the classified defects is displayed (figure 3 numeral 340).

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claim 30 rejected under 35 U.S.C. 103(a) as being unpatentable over Gallarda et al. USPN 6,539,106 in view of Somekh et al. USPN 6,763,130 (hereinafter "Somekh").

Claim 30 depends on claim 28 and further discloses that data regarding the masked region is also output. Gallarda does not explicitly disclose that data regarding the masked region (the region covered by the feature template extraction unit) is output, however Gallarda does disclose that a defect map is output (figure 3 numeral 345). It is well known to output a defect map that includes a view of the entire wafer as well the mapping of the defects on the wafer. Somekh et al. USPN 6,763,130 discloses a wafer defect map where the entire wafer is shown (figure 4). If the entire wafer is shown then data regarding the masked region is also shown.

Gallarda and Somekh are analogous art because they are from the same field of endeavor of wafer inspection using image processing.

At the time of the invention it would have been obvious to one of ordinary skill in the art to display the entire wafer in the defect map (and thus to output areas that have been masked by Gallarda) in order to give the operator a clear idea of where the defects are. Thus it would have been obvious to one of ordinary skill in the art to combine Gallarda and Somekh to obtain the invention as specified in claim 30.

8. Claims 31-37 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gallarda et al. USPN 6,539,106 in view of Matsui et al. USPN 5,850,467 (hereinafter "Matsui").

Gallarda discloses a pattern inspection method comprising the steps of: attaining a digital image of an object substrate through microscopic observation thereof (col. 3 lines 23-29, and col. 16 lines 27-34 disclose that the test image can be from a scanning-electron-microscope); detecting defects of a pattern formed on said object substrate by comparing said digital image with a reference image stored in a memory; and displaying data on the defects detected on a display screen (figure 3 numeral 345); wherein at the step of displaying a positional distribution of the defects on said object substrate is displayed on the display screen while excluding defects having a feature that matches with a pre-registered feature or distinguishing from defects which do not have a feature that matches with the pre-registered feature (col. 3 lines 19-55 disclose preparing a reference image and a test image, extracting features from the reference image and extracting features from the test image, and comparing features of the reference image and of the test image to identify defects, wherein the extracting features from an image can comprise matching a feature template in the image and identifying features in the image that match the feature-template [thus excluding nuisance defects having a feature that matches with a pre-registered feature], figure 3 numeral 345 discloses a display for outputting a defect map, defect location, size, type, etc.). This leads to a reduced rate of nuisance defects and false defects, and increased sensitivity to killer defects (col. 5 lines 45-50).

Gallarda does not explicitly disclose displaying an enlarged image of a defect among the defects detected. Matsui discloses that it is difficult to detect an extremely small defect when inspecting a reticle (col. 2 lines 41-50). To remedy this problem Matsui discloses enlarging the defect such as seen in figures 4a and 4c (col. 5 lines 11-17). This enables for very small defects to be detected.

Gallarda and Matsui are analogous art because they are from the same field of endeavor of semiconductor inspection using image processing.

At the time of the invention it would have been obvious to one of ordinary skill in the art to modify Gallarda to display an enlarged image of a defect. The motivation for doing so is that it would make it easier for the operator to detect the small defects. Thus it would have been obvious to one of ordinary skill in the art to combine Gallarda and Matsui to obtain the invention as specified in claim 31.

Regarding claim 32, Gallarda discloses that the reference image and test image can be obtained using a scanning-electron-microscope (col. 16 line10-34) and a feature template can be used to aid in the feature extraction for a particular type of image can be used to extract the features (col. 17 lines 45-59), thus it is inherent that if the feature template is to be used with a microscopic reference and test images then it must be set up using a microscopic image.

Regarding claim 33, Gallarda discloses a defect map thus displaying the defect on the display (figure 3 numeral 345).

Claim 34 is similar to claim 31 with the extra limitation that data regarding defects located in a preregistered area is output so as to be distinguishable from data regarding

an other detected defect. Gallarda discloses displaying a map of defects and their positional data (figure 3 numeral 345, and col. 6 lines 32-35). As the display is a map it is possible to distinguish one defect from another defect based on its position on the map.

Regarding claim 35, Gallarda discloses that the reference image and test image can be obtained using a scanning-electron-microscope (col. 16 line10-34) and a feature template can be used to aid in the feature extraction for a particular type of image can be used to extract the features (col. 17 lines 45-59), thus it is inherent that if the feature template is to be used with a microscopic reference and test images then it must be set up using a microscopic image.

Regarding claim 36, positional data of the defects is displayed on a display screen with an image of the other detected defects (figure 3 numeral 345).

Regarding claim 37, feature data includes defect position (figure 3 numeral 345).

9. Claims 41-42 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gallarda et al. USPN 6,539,106 in view of Ikenega USPN 4,989,156.

Gallarda does not explicitly disclose that the feature quantity is displayed on a CAD terminal, however does discuss that the feature data is outputted for an operator (col. 6 lines 30-35) and furthermore that the reference data can come from CAD data (col. 16 lines 10-26).

It is well known to display design information to CAD so that it may be modified by an operator. Ikenaga discloses outputting CAD data so that an operator can visually check a wafer pattern and then modify the data (col. 4 lines 24-42).

Gallarda and Ikenaga are analogous art because they are both from the same field of endeavor of semiconductor design.

At the time of the invention it would have been obvious to display the defect map on a CAD terminal to allow the operator to make design changes. Thus it would have been obvious to one of ordinary skill in the art to combine Gallarda and Ikenaga to obtain the invention of claims 41-42.

Conclusion

10. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Contact Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to John B. Strege whose telephone number is (571) 272-7457. The examiner can normally be reached on Monday-Friday between the hours of 8-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Bhavesh Mehta can be reached on (571) 272-7453. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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